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Single Touch Single ouput Touch IC

Document：PT-DS21007

1. General Description

PT2041A is a single channel touch control ASIC, which built-in LDO circuit to provide a stable voltage for the touch sensing circuit. At the same time, the chip has high efficient touch detection algorithm, supply a stable touch detection effect. The chip is designed to replace the traditional keys, with advantages of wide operating voltage and low power consumption, and it has been widely studied and applied.

2. Main Features

- Power supply range：2.4~5.5V
- Working temperature range: -40~85℃
- Good anti-interference performance, e.g., built in LDO circuit, power on reset, low-voltage reset function, environment adaptive algorithm
- Standby current:2uA@V_{DD}=3V/no load
- The longest response time of key: about 200ms@V_{DD}=3V in low power consumption mode
- External capacitance(1~50pF) can be connected to adjust the touch sensitivity.
- Output mode selection (TOG): synchronous output or toggle output
- CMOS output (QC) effective level selection(AHLB): Active High/Low.
- Maximum output time of key: 16 seconds (± 30%)
- The initialization time of power on is about 0.4 seconds. During this period, do not touch the detection point, and all functions are prohibited currently.
- HBM ESD > 4KV
- Package Types: SOT23-6、DFN2*2-6L、DFN1*1-4L
- It can not be used in application scenarios where the resistance and capacitance are reduced and the power ripple is too large. Applicable only to battery-powered applications with less ripple power supply. PT2022T6 is a good choice for applications with high anti-jamming capability.

3. System Block Diagram

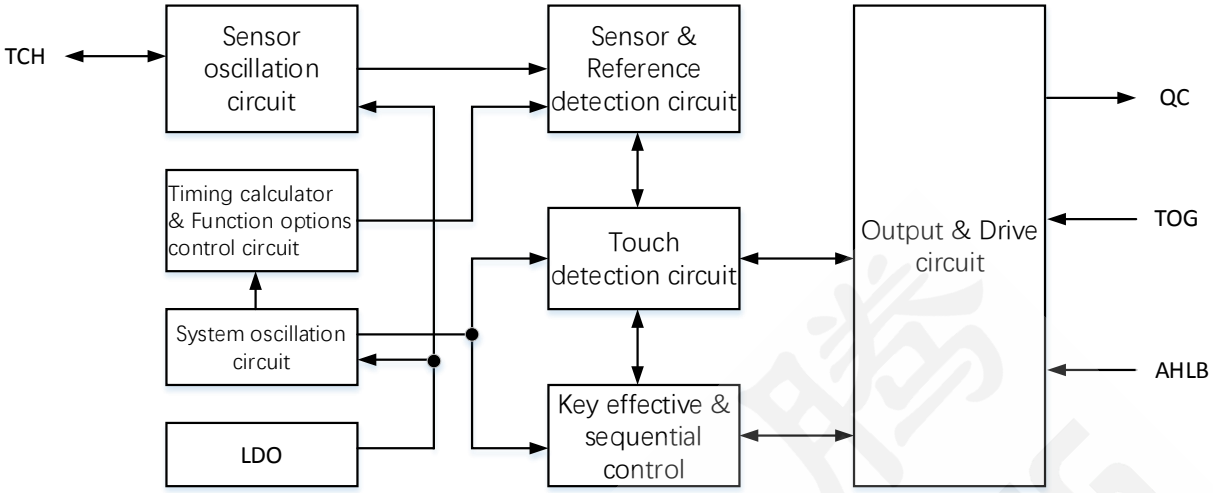


Figure1 System block diagram

4. Package and Pin Description

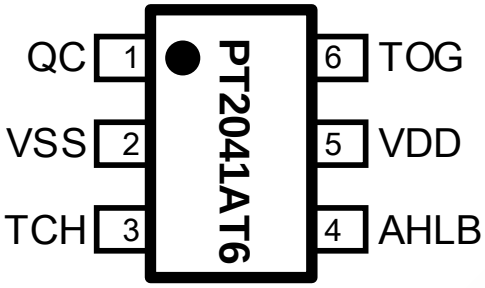


Figure2 SOT23-6 package

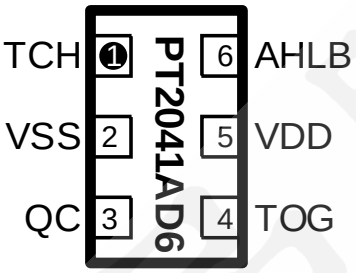


Figure3 DFN2x2-6L package

Note: Pin layout and SOT23-6 reverse

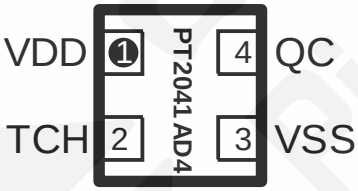


Figure4 DFN1x1-4L package

Note: Fixed to synchronous output mode, output high level effective

Table1 pin description

NO.			Pin name	I/O	Description
SOT23-6	DFN2x2-6L	DFN1x1-4L			
1	3	4	QC	O	Output Pin，CMOS output
2	2	3	VSS	P	Negative power supply
3	1	2	TCH	I	Touch input pad
4	6	/	AHLB	I-PL	Output level selection: 0：High level active(default) 1：Low level active
5	5	1	VDD	P	Positive power supply
6	4	/	TOG	I-PL	output mode select: 0：Synchronous output(default) 1：Toggle output

Pin types:

I： CMOS input　　O：CMOS output　　I/O：CMOS input/output　　P：Power/ground

I-PH：CMOS Input built-in pull-up resistor　　I-PL：CMOS Input built-in pull-down resistor

5. Function Description

5.1 Ouput mode and option pin

The pins of AHLB and TOG are latch type: the default state of power on is 0. If the pins are connected to VDD before power on, the state will change to 1 after power on, and there will be no current leakage.

TOG pin: select synchronous output or toggle output.

AHLB pin: select CMOS output high level valid or low level valid.

QC pin (CMOS output) option features:

TOG	AHLB	Port QC option features
0	0	Synchronous mode, CMOS high level active
0	1	Synchronous mode, CMOS low level active
1	0	Toggle output, power on state = 0
1	1	Toggle output, power on state = 1

5.2 Maximum output time of key

If there is an object covering the touch pad or the environment changes suddenly, the touch detection may continue to be effective. When the IC internal touch algorithm detects that the output effective duration reaches the set value of 16S (± 30%), the system will return to the initial power on state, and the output becomes invalid.

5.3 Low power mode

PT2041A runs in low power consumption mode, which can save power consumption. In this mode, when the key touch is detected, it will switch to fast mode until the key touch is released, and maintain fast mode for about 10 seconds, and then return to low power consumption mode.

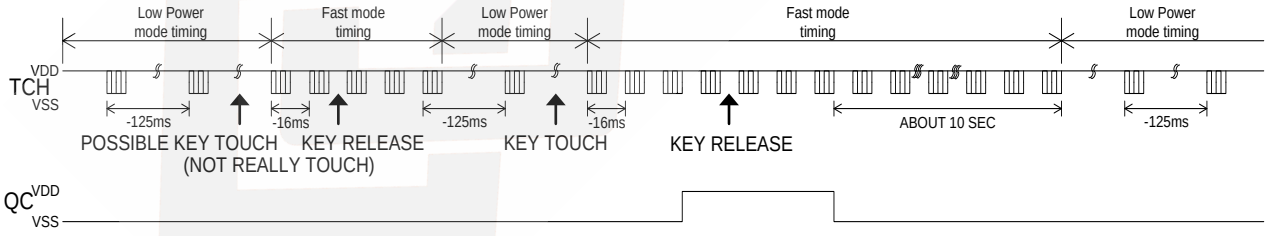


Figure 5 Time Series Diagram

5.4 Sensitivity adjustment

The equivalent capacitance on the IC touch pin will affect the sensitivity. The sensitivity adjustment must conform to the practical application of PCB. Here are some methods to adjust the sensitivity:

1) Adjust the size of the touch pad:
   When other conditions remain unchanged, using a larger size of the touch pad can increase the sensitivity, otherwise it will reduce the sensitivity; but the size of the touch pad must be within the effective range.
2) Adjust the thickness of the media panel:
   When other conditions remain unchanged, the use of thinner media can increase the sensitivity, otherwise it will decrease the sensitivity.

3) Adjust C_S capacitance value

When other conditions remain unchanged, the sensitivity is the highest when there is no grounded C_S capacitance on the touch pad, otherwise, the higher the C_S capacitance is, the lower the sensitivity will be. The available range of C_S capacitance is: ($1 \leqslant C_S \leqslant 50pF$).

6. Application Circuit

Cm reserves capacitance for PT2022T6 and can be directly replaced with PT2022T6 if anti-jamming capability is not satisfied.

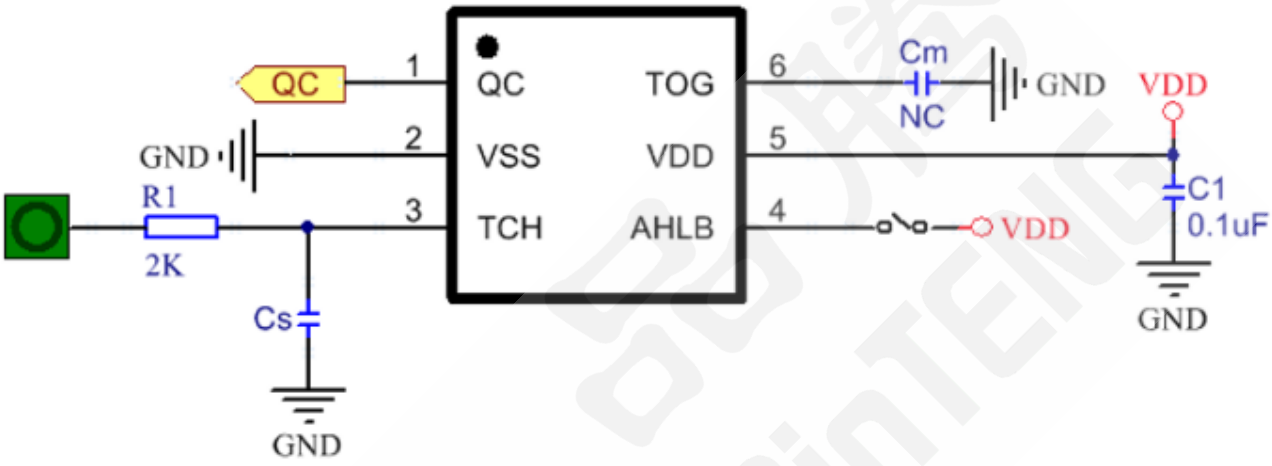


Figure 6 Standard application circuit

Special Notes:

1) On PCB, the shorter the line from touch pad to TCH pin is, the better. The touch line should not be parallel or cross with other lines.

2) The power supply must be stable. If the power supply voltage drifts or jumps rapidly, it may cause abnormal sensitivity or false detection.

3) The medium covered on PCB shall not contain metal or conductive components, and the surface coating shall also meet the same requirements.

4) C1 capacitor (104 or more) must be used between Vdd and GND, and the shortest distance between Vdd and GND pins of IC should be adopted.

5) C_S capacitance can be used to adjust the sensitivity. The smaller the C_S capacitance is, the higher the sensitivity is. The sensitivity must be adjusted according to the practical PCB. The range of C_S capacitance is 1 ~ 50pF.

6) To adjust the sensitivity of the capacitor (C_S), smaller temperature coefficient and more stable capacitor must be selected, such as X7R, NPO. For touch applications, it is recommended to select NPO capacitors to reduce the sensitivity due to temperature changes.

7. Electrical Characteristics

7.1 limit parameters of electrical characteristics

Table 2 limit parameters

Parameters	Lable	Condition	Range	Unit
Power supply voltage	V_{DD}	-	-0 to +5.5	V
Input voltage	V_I	all I/O	-0.3 to V_{DD}+0.3	V
working temperature	T_A	-	-40~ +85	℃
Storage temperature	T_{STG}	-	-50~ +125	℃
HBM	ESD		4	KV

7.2 DC characteristics

Table 3 DC characteristics（Unless otherwise specified V_{DD} = 2.4V~5.5V，Temp = 25ºC）

Parameter	Lable	Condition	Min	Typ	Max	Unit
Working voltage	V_{DD}		2.4	3	5.5	V
Input high voltage threshold	V_{IH}	V_{DD}=5V,AHLB	0.75*VDD		1.0*VDD	V
		V_{DD}=5V,TOG	0.4*VDD		1.0*VDD	
Input low voltage threshold	V_{IL}	V_{DD}=5V,AHLB	0		0.25*VDD	V
		V_{DD}=5V,TOG	0		0.15*VDD	
Output current of Source	I_{OH}	V_{DD}=3V, VOH=2.1V		2		mA
Output current of Sink	I_{OL}	V_{DD}=3V, VOL=0.9V		15		mA
Pull down resistance	R_{PL}	V_{DD}=3V, Fast mode	24	30	36	Kohm
Output response time	T_R	V_{DD}=3V, Low power mode			40	ms
		V_{DD}=3V, Low power mode (no load)			200	
Standby current	I_{SB}	V_{DD}=3V, Fast mode (no load)		2	2.5	uA
		V_{DD}=3V, Fast mode		20	25	

8. Package Outline

8.1 SOT23-6 Package

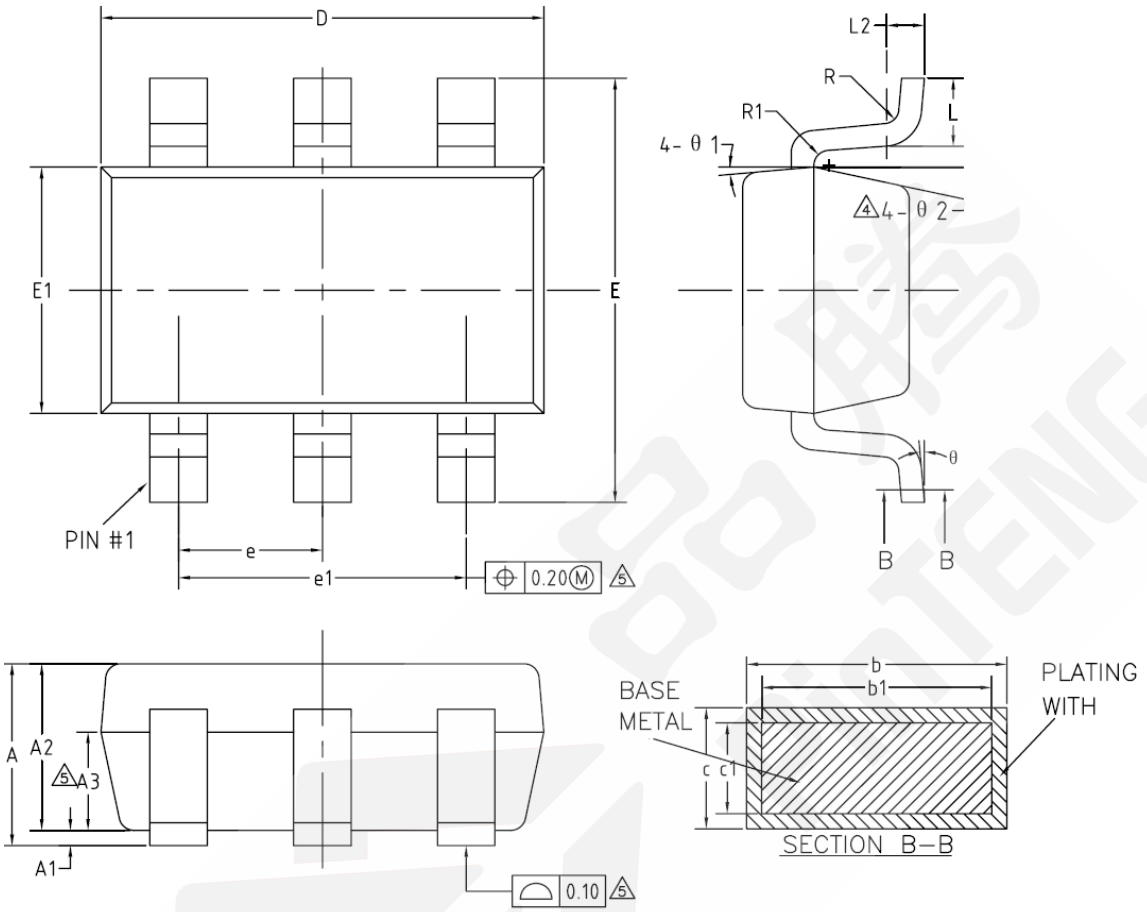


Figure 7 SOP23-6 Package

Table 4 SOP23-6 Package size

Unit: mm

Symbol	Min	Typ	Max		Symbol	Min	Typ	Max
A	-	-	1.25		e	0.90	0.95	1.00
A1	0	-	0.15		e1	1.80	1.90	2.00
A2	1.00	1.10	1.20		L	0.35	0.45	0.60
A3	0.60	0.65	0.70		L1	0.59RET		
B	0.36	-	0.50		L2	0.25BSC		
b1	0.36	0.38	0.45		R	0.10	-	-
C	0.14	-	0.20		R1	0.10	-	0.20
c1	0.14	0.15	0.16		θ	0	-	8°
D	2.826	2.926	3.026		θ1	3°	5°	7°
E	2.60	2.80	3.00		θ2	6°	-	14°
E1	1.526	1.626	1.726					

8.2 DFN2x2-6L Package

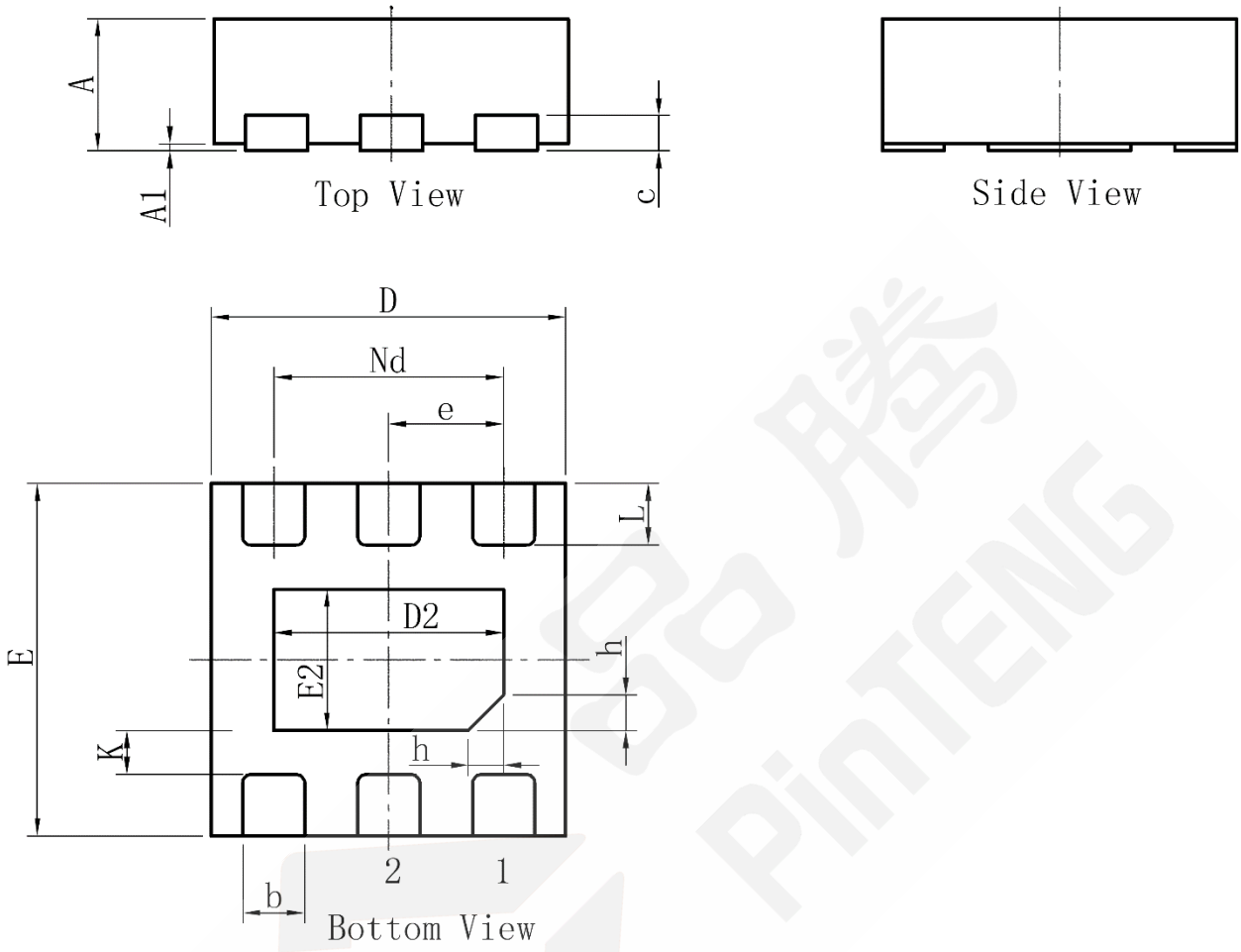


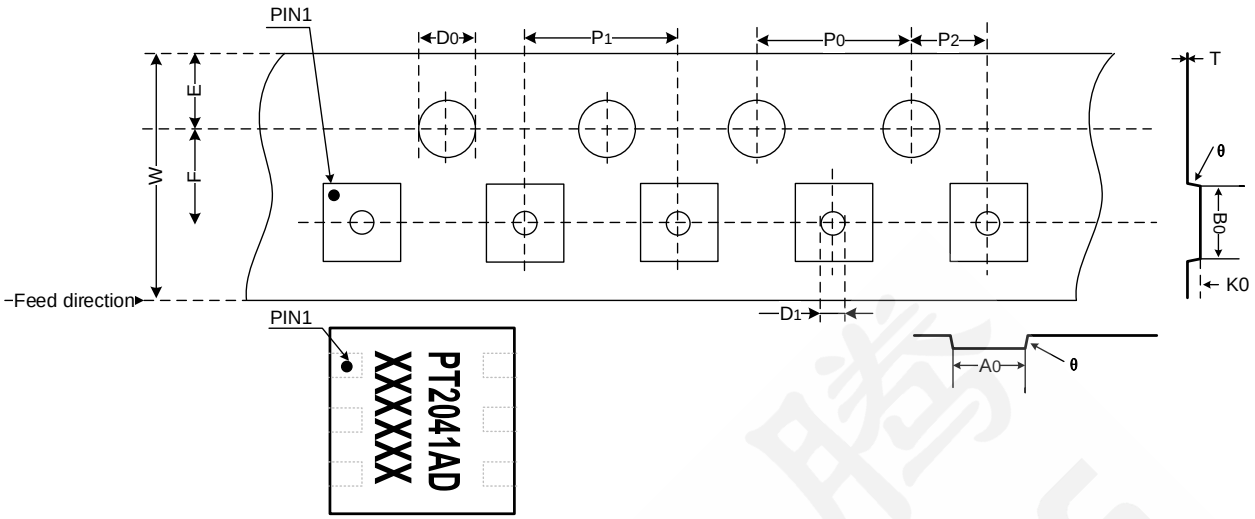
Figure 8 DFN2x2-6L Package

Table 5 DFN2x2-6L Package Size

Unit: mm

Symbol	Min	Typ	Max		Symbol	Min	Typ	Max
A	0.70	0.75	0.80		E2	0.75	0.80	0.85
A1	0.00	0.02	0.05		e	0.650BSC		
b	0.30	0.35	0.40		Nd	1.300BSC		
c	0.18	0.20	0.25		K	0.20	-	-
D	1.95	2.00	2.05		L	0.28	0.33	0.38
D2	1.25	1.30	1.35		h	0.15	0.20	0.25
E	1.95	2.00	2.05					

8.3 DFN2x2-6L Taping Information



DFN2*2-6L Seal Example

Figure 9 DFN2x2-6L Taping example

Table 6 DFN2x2-6L Taping Size

Unit: mm

Symbol	Min	Typ	Max		Symbol	Min	Typ	Max
W	7.9	8.00	8.10		D1	-	1.00	1.10
A0	2.15	2.25	2.35		D0	-	1.50	1.60
B0	2.15	2.25	2.35		P0	3.90	4.00	4.10
K0	0.85	0.95	1.05		P1	3.90	4.00	4.10
E	1.65	1.75	1.85		P2	1.90	2.00	2.10
F	3.40	3.50	3.60		T	0.20	0.22	0.24
					θ		10°	

8.4 DFN1x1-4L Package

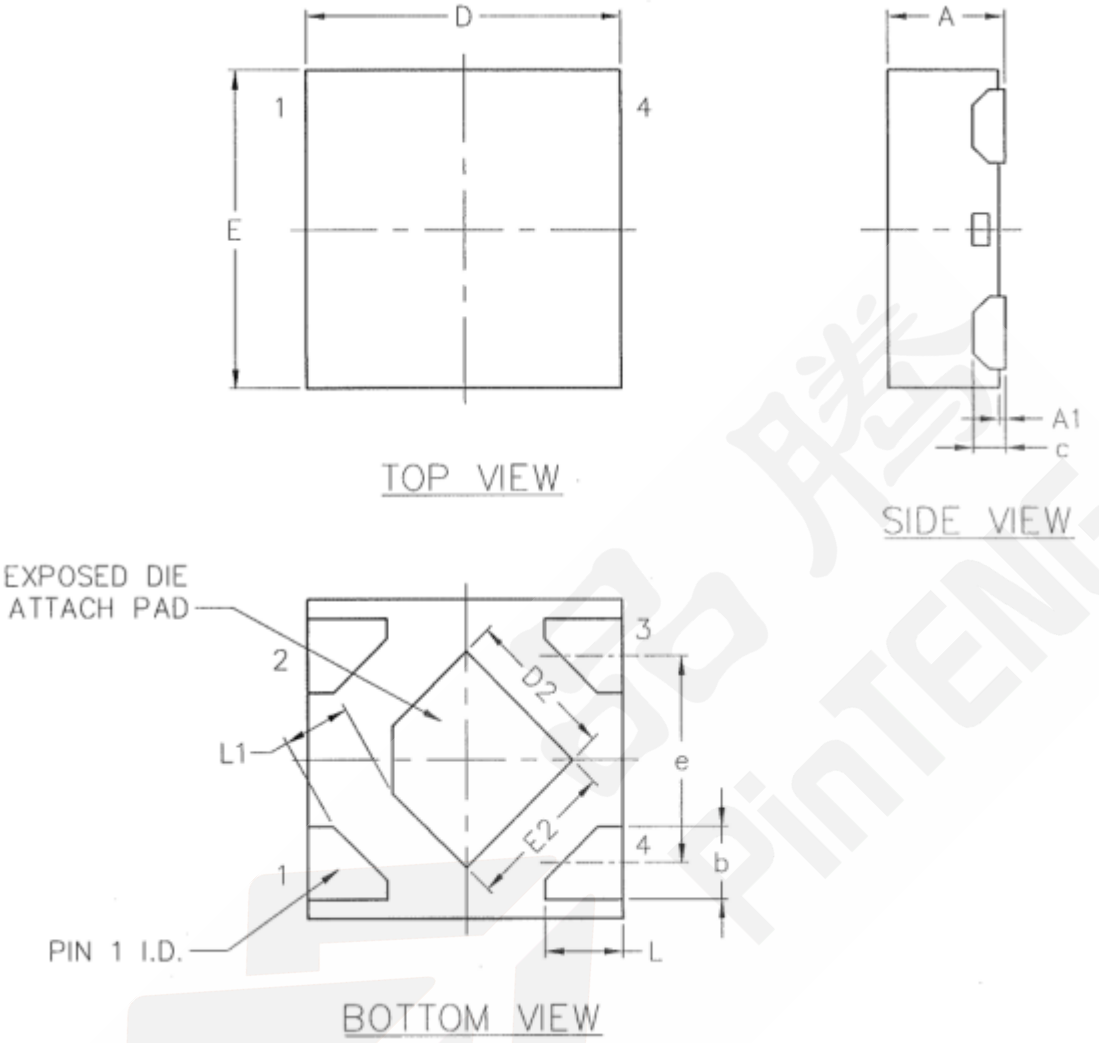


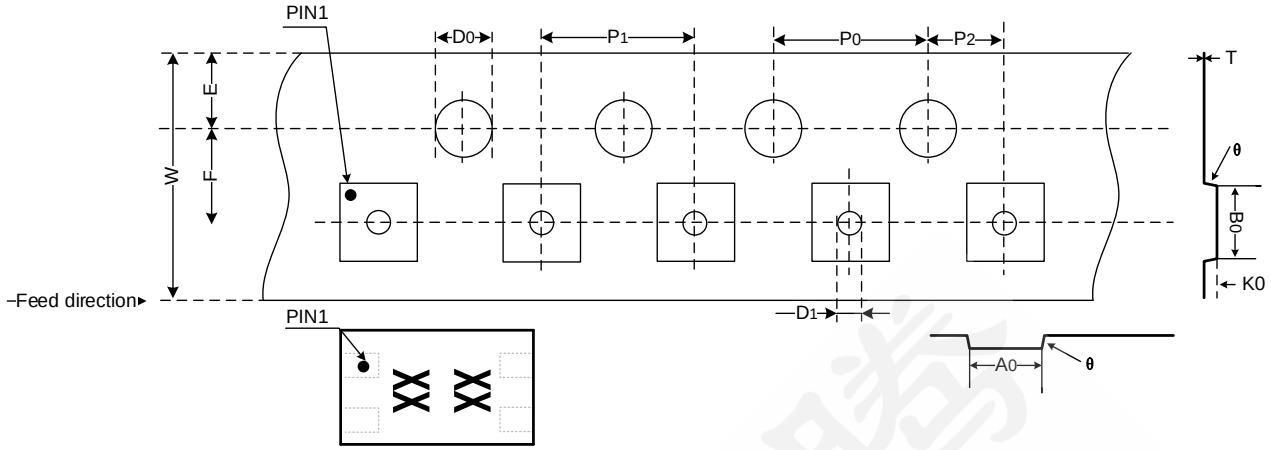
Figure 10 DFN1x1-4L Package

Table 7 DFN1x1-4L Package Size

Unit: mm

Symbol	Min	Typ	Max		Symbol	Min	Typ	Max
A	0.32	0.37	0.40		E2	0.43	0.48	0.53
A1	0.00	0.02	0.05		e	0.650 BSC		
b	0.18	0.23	0.28		L1	0.205 REF		
c	0.102 REF				E	0.95	1.00	1.05
D	0.95	1.00	1.05		L	0.20	0.25	0.30
D2	0.43	0.48	0.53					

8.5 DFN1x1-4L Taping Information



DFN1*1-4L Seal Example

Figure 11 DFN1x1-4L Taping example

表 8 DFN1x1-4L Taping size

Unit: mm

Symbol	Min	Typ	Max		Symbol	Min	Typ	Max
W	7.9	8.00	8.10		D1	-	0.7	0.8
A0	1.15	1.25	1.35		D0	-	1.50	1.60
B0	1.15	1.25	1.35		P0	3.90	4.00	4.10
K0	0.47	0.57	0.67		P1	3.90	4.00	4.10
E	1.65	1.75	1.85		P2	1.90	2.00	2.10
F	3.40	3.50	3.60		T	0.18	0.23	0.28
					θ		6°	

9. History

Version	Modification record	Release Time
V1.0	Initial version	2021-06-09
V1.1	Update DFN1*1-4L package description	2021-09-23
V1.2	Update HBM ESD parameters	2022-05-30
V1.3	Add application considerations	2022-07-21
V1.4	Update Typical Application Circuits	2023-03-14

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